COMS10015 lab. worksheet #5 + #7

Although some questions have a written solution below, for others it will be more useful to experiment in a hands-on manner (e.g., using a concrete implementation). The file

https://assets.phoo.org/COMS10015_2025_TB-4/csdsp/sheet/lab-07_s.tar.gz

supports such cases.

§1. C-class, or core questions

▷ **S1[C].** An associated solution, i.e., a (documented) implementation, for this question can be found in the archive provided. Note that one can produce such a solution by taking content from the lecture slot(s), then translating (or "porting") it into a Verilog implementation: for reference, Figure 1 captures that content.

▷ **S2[C].** An associated solution, i.e., a (documented) implementation, for this question can be found in the archive provided.

▷ **S3[C].** An associated solution, i.e., a (documented) implementation, for this question can be found in the archive provided.

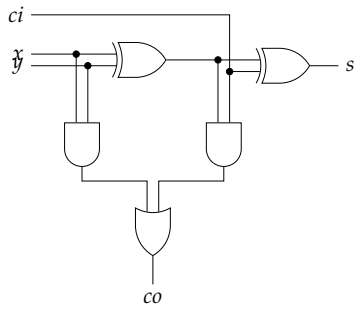
§2. R-class, or revision questions

▷ **S4[R].** There is a set of solutions available at

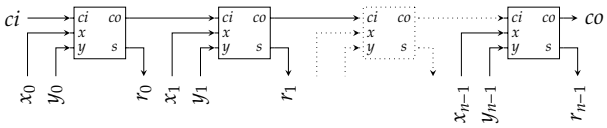
https://assets.phoo.org/COMS10015_2025_TB-4/csdsp/sheet/misc-revision_s.pdf

§3. A-class, or additional questions

▷ **S5[A].** There is no associated solution for this question, because it is somewhat open-ended with respect to 1) the goal or challenge presented, and/or 2) the assumptions and decisions you make, and therefore the design space of viable solutions.



(a) *A* 1*-bit full-adder design.*



(b) *An* n*-bit ripple-carry adder design.*

Figure 1: *Diagrammatic* 1*- and* n*-bit adder designs.*