## COMS10015 quick(ish) reference hand-out: transistors and logic gates

## Definition: informal

**N-MOSFET** : 
$$g \longrightarrow \begin{cases} g = V_{dd} = 5V \Rightarrow \text{ transistor is activated, } s \text{ and } d \text{ connected} \\ g = V_{ss} \simeq GND = 0V \Rightarrow \text{ transistor is deactivated, } s \text{ and } d \text{ disconnected} \end{cases}$$

**P-MOSFET** : 
$$g \rightarrow \begin{bmatrix} s \\ g = V_{ss} \simeq GND = 0V \Rightarrow \text{ transistor is activated, } s \text{ and } d \text{ connected } g = V_{dd} = 5V \Rightarrow \text{ transistor is deactivated, } s \text{ and } d \text{ disconnected } d \text{ disconnected } s \text{ and } s \text{$$

## **Definition:** formal

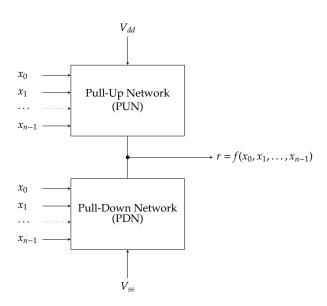
**Definition 1.** An **N-MOSFET** (or **N-type MOSFET**, or **N-channel MOSFET**, or **NPN MOSFET**) is constructed from *N-type semi-conductor terminals and a P-type body:* 

- applying a potential difference to the gate widens the conductive channel, meaning source and drain are connected (i.e., act like a conductor); the transistor is activated.
- removing the potential difference from the gate narrows the conductive channel, meaning source and drain are disconnected (i.e., act like an insulator); the transistor is deactivated.

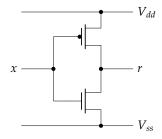
**Definition 2.** A **P-MOSFET** (or **P-type MOSFET**, or **P-channel MOSFET**, or **PNP MOSFET**) is constructed from *P-type semi-conductor terminals and an N-type body:* 

- applying a potential difference to the gate narrows the conductive channel, meaning source and drain are disconnected (i.e., act like an insulator); the transistor is deactivated.
- removing the potential difference from the gate widens the conductive channel, meaning source and drain are connected (i.e., act like a conductor); the transistor is activated.

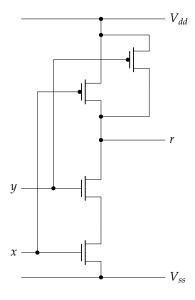
## Design framework



Logic gates: NOT



Logic gates: NAND



Logic gates: NOR

