

Computer Architecture

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Keep in mind there are *two* PDFs available (of which this is the latter):

1. a PDF of examinable material used as lecture slides, and
2. a PDF of non-examinable, extra material:
 - ▶ the associated notes page may be pre-populated with extra, written explanation of material covered in lecture(s), plus
 - ▶ anything with a “grey’ed out” header/footer represents extra material which is useful and/or interesting but out of scope (and hence not covered).

Notes:

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► **Concept:** consider

$$\begin{array}{lcl} \hat{x} & \mapsto & x \\ \hat{y} & \mapsto & y \end{array}$$

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$$\begin{array}{lcl} \hat{x} & \mapsto & x \\ \hat{y} & \mapsto & y \\ \hat{r} & \mapsto & r = x + y \end{array}$$

Notes:

► **Concept:** consider

$$\begin{array}{rcl} \hat{x} & \mapsto & x \\ \hat{y} & \mapsto & y \\ f(\hat{x}, \hat{y}) = \hat{r} & \mapsto & r = x + y \end{array}$$

where f

1. has an action on $\hat{x}$ and $\hat{y}$ compatible with that of $+$ on x and y :

- accepts n -bit
 - **addend** $\hat{x}$, and
 - **addend** $\hat{y}$

as input, and

- produces an $(n + 1)$ -bit **sum** $\hat{r}$ as output,

2. is a Boolean function:

$$f : \{0, 1\}^n \times \{0, 1\}^n \rightarrow \{0, 1\}^{n+1}$$

Notes:

► **Agenda:** produce a design(s) for f , which

1. functions correctly, and
2. satisfies pertinent quality metrics (e.g., is efficient in time and/or space).

Notes:

ARMv8-Advs with Legacy <table> <tr> <th>Instruction</th><th>Op</th><th>Op2</th><th>Op3</th><th>Op4</th><th>Op5</th><th>Op6</th><th>Op7</th><th>Op8</th><th>Op9</th><th>Op10</th><th>Op11</th><th>Op12</th><th>Op13</th><th>Op14</th><th>Op15</th><th>Op16</th><th>Op17</th><th>Op18</th><th>Op19</th><th>Op20</th><th>Op21</th><th>Op22</th><th>Op23</th><th>Op24</th><th>Op25</th><th>Op26</th><th>Op27</th><th>Op28</th><th>Op29</th><th>Op30</th><th>Op31</th><th>Op32</th><th>Op33</th><th>Op34</th><th>Op35</th><th>Op36</th><th>Op37</th><th>Op38</th><th>Op39</th><th>Op40</th><th>Op41</th><th>Op42</th><th>Op43</th><th>Op44</th><th>Op45</th><th>Op46</th><th>Op47</th><th>Op48</th><th>Op49</th><th>Op50</th><th>Op51</th><th>Op52</th><th>Op53</th><th>Op54</th><th>Op55</th><th>Op56</th><th>Op57</th><th>Op58</th><th>Op59</th><th>Op60</th><th>Op61</th><th>Op62</th><th>Op63</th><th>Op64</th><th>Op65</th><th>Op66</th><th>Op67</th><th>Op68</th><th>Op69</th><th>Op70</th><th>Op71</th><th>Op72</th><th>Op73</th><th>Op74</th><th>Op75</th><th>Op76</th><th>Op77</th><th>Op78</th><th>Op79</th><th>Op80</th><th>Op81</th><th>Op82</th><th>Op83</th><th>Op84</th><th>Op85</th><th>Op86</th><th>Op87</th><th>Op88</th><th>Op89</th><th>Op90</th><th>Op91</th><th>Op92</th><th>Op93</th><th>Op94</th><th>Op95</th><th>Op96</th><th>Op97</th><th>Op98</th><th>Op99</th><th>Op100</th><th>Op101</th><th>Op102</th><th>Op103</th><th>Op104</th><th>Op105</th><th>Op106</th><th>Op107</th><th>Op108</th><th>Op109</th><th>Op110</th><th>Op111</th><th>Op112</th><th>Op113</th><th>Op114</th><th>Op115</th><th>Op116</th><th>Op117</th><th>Op118</th><th>Op119</th><th>Op120</th><th>Op121</th><th>Op122</th><th>Op123</th><th>Op124</th><th>Op125</th><th>Op126</th><th>Op127</th><th>Op128</th><th>Op129</th><th>Op130</th><th>Op131</th><th>Op132</th><th>Op133</th><th>Op134</th><th>Op135</th><th>Op136</th><th>Op137</th><th>Op138</th><th>Op139</th><th>Op140</th><th>Op141</th><th>Op142</th><th>Op143</th><th>Op144</th><th>Op145</th><th>Op146</th><th>Op147</th><th>Op148</th><th>Op149</th><th>Op150</th><th>Op151</th><th>Op152</th><th>Op153</th><th>Op154</th><th>Op155</th><th>Op156</th><th>Op157</th><th>Op158</th><th>Op159</th><th>Op160</th><th>Op161</th><th>Op162</th><th>Op163</th><th>Op164</th><th>Op165</th><th>Op166</th><th>Op167</th><th>Op168</th><th>Op169</th><th>Op170</th><th>Op171</th><th>Op172</th><th>Op173</th><th>Op174</th><th>Op175</th><th>Op176</th><th>Op177</th><th>Op178</th><th>Op179</th><th>Op180</th><th>Op181</th><th>Op182</th><th>Op183</th><th>Op184</th><th>Op185</th><th>Op186</th><th>Op187</th><th>Op188</th><th>Op189</th><th>Op190</th><th>Op191</th><th>Op192</th><th>Op193</th><th>Op194</th><th>Op195</th><th>Op196</th><th>Op197</th><th>Op198</th><th>Op199</th><th>Op200</th><th>Op201</th><th>Op202</th><th>Op203</th><th>Op204</th><th>Op205</th><th>Op206</th><th>Op207</th><th>Op208</th><th>Op209</th><th>Op210</th><th>Op211</th><th>Op212</th><th>Op213</th><th>Op214</th><th>Op215</th><th>Op216</th><th>Op217</th><th>Op218</th><th>Op219</th><th>Op220</th><th>Op221</th><th>Op222</th><th>Op223</th><th>Op224</th><th>Op225</th><th>Op226</th><th>Op227</th><th>Op228</th><th>Op229</th><th>Op230</th><th>Op231</th><th>Op232</th><th>Op233</th><th>Op234</th><th>Op235</th><th>Op236</th><th>Op237</th><th>Op238</th><th>Op239</th><th>Op240</th><th>Op241</th><th>Op242</th><th>Op243</th><th>Op244</th><th>Op245</th><th>Op246</th><th>Op247</th><th>Op248</th><th>Op249</th><th>Op250</th><th>Op251</th><th>Op252</th><th>Op253</th><th>Op254</th><th>Op255</th><th>Op256</th><th>Op257</th><th>Op258</th><th>Op259</th><th>Op260</th><th>Op261</th><th>Op262</th><th>Op263</th><th>Op264</th><th>Op265</th><th>Op266</th><th>Op267</th><th>Op268</th><th>Op269</th><th>Op270</th><th>Op271</th><th>Op272</th><th>Op273</th><th>Op274</th><th>Op275</th><th>Op276</th><th>Op277</th><th>Op278</th><th>Op279</th><th>Op280</th><th>Op281</th><th>Op282</th><th>Op283</th><th>Op284</th><th>Op285</th><th>Op286</th><th>Op287</th><th>Op288</th><th>Op289</th><th>Op290</th><th>Op291</th><th>Op292</th><th>Op293</th><th>Op294</th><th>Op295</th><th>Op296</th><th>Op297</th><th>Op298</th><th>Op299</th><th>Op300</th><th>Op301</th><th>Op302</th><th>Op303</th><th>Op304</th><th>Op305</th><th>Op306</th><th>Op307</th><th>Op308</th><th>Op309</th><th>Op310</th><th>Op311</th><th>Op312</th><th>Op313</th><th>Op314</th><th>Op315</th><th>Op316</th><th>Op317</th><th>Op318</th><th>Op319</th><th>Op320</th><th>Op321</th><th>Op322</th><th>Op323</th><th>Op324</th><th>Op325</th><th>Op326</th><th>Op327</th><th>Op328</th><th>Op329</th><th>Op330</th><th>Op331</th><th>Op332</th><th>Op333</th><th>Op334</th><th>Op335</th><th>Op336</th><th>Op337</th><th>Op338</th><th>Op339</th><th>Op340</th><th>Op341</th><th>Op342</th><th>Op343</th><th>Op344</th><th>Op345</th><th>Op346</th><th>Op347</th><th>Op348</th><th>Op349</th><th>Op350</th><th>Op351</th><th>Op352</th><th>Op353</th><th>Op354</th><th>Op355</th><th>Op356</th><th>Op357</th><th>Op358</th><th>Op359</th><th>Op360</th><th>Op361</th><th>Op362</th><th>Op363</th><th>Op3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Notes:

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Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)				
x	$=$	$107_{(10)}$	$\mapsto$	$1 \ 0 \ 7$
y	$=$	$14_{(10)}$	$\mapsto$	$\underline{0 \ 1 \ 4} \ +$
c	$=$			
r	$=$			

Example ($b = 2$)

x	$=$	$107_{(10)}$	$\mapsto$	$0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1$
y	$=$	$14_{(10)}$	$\mapsto$	$0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0 +$
c	$=$			
r	$=$			

1. this process matches our understanding of manual, “school-book” addition, *and*
2. the same process applies, irrespective of b .

Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 1 & 0 & 7 \\ y & = & 14_{(10)} & \mapsto & 0 & 1 & 4 & + \\ c & = & & & \hline & & & & 0 \\ r & = & & & \hline & & & & \end{array}$$

Example ($b = 2$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ y & = & 14_{(10)} & \mapsto & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & + \\ c & = & & & \hline & & & & & & & & & & \\ r & = & & & \hline & & & & & & & & & & \end{array}$$

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Notes:

Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

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Example ($b = 2$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ y & = & 14_{(10)} & \mapsto & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & + \\ c & = & & & \hline & & & & & & & & & \\ r & = & & & \hline & & & & & & & & & \end{array}$$

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Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 1 & 0 & 7 \\ y & = & 14_{(10)} & \mapsto & 0 & 1 & 4 & + \\ c & = & & & 0 & 1 & 0 \\ r & = & & & 2 & 1 \end{array}$$

Example ($b = 2$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ y & = & 14_{(10)} & \mapsto & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & + \\ c & = & & & & & & & & & & \\ r & = & & & & & & & & & & \end{array}$$

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Notes:

Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 1 & 0 & 7 \\ y & = & 14_{(10)} & \mapsto & 0 & 1 & 4 & + \\ c & = & & & 0 & 0 & 1 & 0 \\ r & = & 121_{(10)} & \mapsto & 1 & 2 & 1 \end{array}$$

Example ($b = 2$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ y & = & 14_{(10)} & \mapsto & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & + \\ c & = & & & & & & & & & & \\ r & = & & & & & & & & & & \end{array}$$

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$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 \\ y & = & 14_{(10)} & \mapsto & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & + \\ c & = & & & & & & & & & & & \\ r & = & & & & & & & & & & & \end{array}$$

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Notes:

Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto & 1 & 0 & 7 \\ y & = & 14_{(10)} & \mapsto & 0 & 1 & 4 & + \\ c & = & & & 0 & 0 & 1 & 0 \\ r & = & 121_{(10)} & \mapsto & 1 & 2 & 1 \end{array}$$

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1. this process matches our understanding of manual, “school-book” addition, *and*
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Part 1: addition in theory (1)

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Notes:

Part 2: addition in practice: an algorithm (1)

Algorithm

Input: Two unsigned, n -digit, base- b integers x and y , and a 1-digit carry-in $c_i \in \{0, 1\}$
Output: An unsigned, n -digit, base- b integer $r = x + y$, and a 1-digit carry-out $c_o \in \{0, 1\}$

```
1  $r \leftarrow 0, c_0 \leftarrow c_i$ 
2 for  $i = 0$  upto  $n - 1$  step  $+1$  do
3    $r_i \leftarrow (x_i + y_i + c_i) \bmod b$ 
4   if  $(x_i + y_i + c_i) < b$  then  $c_{i+1} \leftarrow 0$  else  $c_{i+1} \leftarrow 1$ 
5 end
6  $CO \leftarrow c_n$ 
7 return  $r, CO$ 
```

Notes:

Part 2: addition in practice: an algorithm (2)

Example

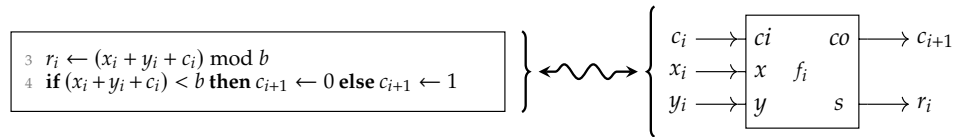
i	x_i	y_i	c_i	r	$x_i + y_i + c_i$	c_{i+1}	r_i	r'
				$\langle 0, 0, 0 \rangle$				$\langle 0, 0, 0 \rangle$
0	7	4	0	$\langle 0, 0, 0 \rangle$	11	1	1	$\langle 1, 0, 0 \rangle$
1	0	1	1	$\langle 1, 0, 0 \rangle$	2	0	2	$\langle 1, 2, 0 \rangle$
2	1	0	0	$\langle 1, 2, 0 \rangle$	1	0	1	$\langle 1, 2, 1 \rangle$
			0	$\langle 1, 2, 1 \rangle$				

Notes:

Part 3: addition in practice: a circuit (1)

► Idea:

- for $b = 2$, it's clear from the algorithm that



- the loop body is therefore analogous to a Boolean function

$$f_i : \{0, 1\}^3 \rightarrow \{0, 1\}^2$$

specified by the following truth table

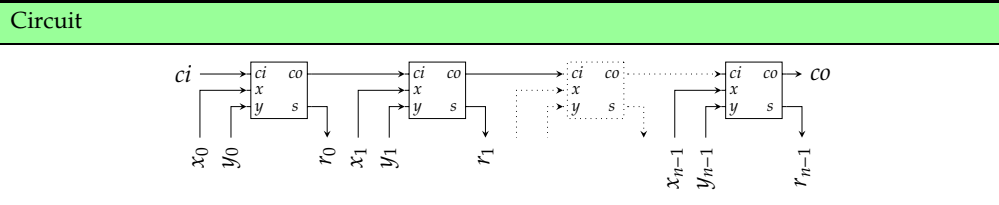
ci	x	y	co	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Notes:

Part 3: addition in practice: a circuit (1)

► Idea:

- the loop bound is fixed, i.e., n is some known constant, so we can unroll it to yield



which, now read left-to-right, mirrors the algorithm:

- the i -th instance f_i implements the i -th loop iteration,
- the connection, or **carry chain** between instances captures c ,
- those instances are termed **full adder** cells,
- this combination of them is termed a **ripple-carry adder**.

Notes:

Part 3: addition in practice: a circuit (2)

► Beware:

- the magnitude of $r = x + y$ can exceed what we can represent via $\hat{r}$:

$\hat{x}$ and $\hat{y}$ are *unsigned*, and there is a carry-out $\Rightarrow$ **carry** condition
 $\hat{x}$ and $\hat{y}$ are *signed*, and the sign of $\hat{r}$ is incorrect $\Rightarrow$ **overflow** condition

- to cope, we typically

1. detect the condition,
2. potentially take some action (e.g., try to “fix” the result somehow),
3. potentially signal the condition somehow (e.g., via a status register or some form of exception).

Notes:

Part 3: addition in practice: a circuit (3)

Example

Consider use of an *unsigned* representation:

$$\begin{array}{rcll} x & = & 15_{(10)} & \mapsto & \begin{array}{cccc} 1 & 1 & 1 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\ c & = & & & \begin{array}{cccc} 1 & 1 & 1 & 1 \end{array} \\ r & = & 0_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 0 \end{array} \end{array} \quad +$$

Here, the carry-out indicates an error: the correct result $r = 16$ is too large for $n = 4$ bits.

► Note that

1. **detection**:

$$\begin{array}{lcl} c_n = CO = 0 & \Rightarrow & \text{no carry} \\ c_n = CO = 1 & \Rightarrow & \text{carry} \end{array}$$

2. **action**, e.g., **truncate** the result to n bits.

Notes:

Part 3: addition in practice: a circuit (4)

Example	Example
Consider use of a <i>signed</i> representation: $\begin{array}{rcll} x & = & -1_{(10)} & \mapsto & \begin{array}{cccc} 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\ c & = & & & \begin{array}{cccc} 1 & 1 & 1 & 0 \end{array} \\ r & = & 0_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 0 \end{array} \end{array} +$ Irrespective of the carry-out, the signs of inputs and output make sense: there is no overflow, so $r = 0$ is correct.	Consider use of a <i>signed</i> representation: $\begin{array}{rcll} x & = & 7_{(10)} & \mapsto & \begin{array}{cccc} 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\ c & = & & & \begin{array}{cccc} 0 & 1 & 1 & 0 \end{array} \\ r & = & -8_{(10)} & \mapsto & \begin{array}{cccc} 1 & 0 & 0 & 0 \end{array} \end{array} +$ Irrespective of the carry-out, the signs of inputs and output make no sense: there is an overflow, so $r = -8$ is incorrect.

► Note that

1. **detection**:

x +ve	y -ve	$\Rightarrow$	no overflow
x -ve	y +ve	$\Rightarrow$	no overflow
x +ve	y +ve	r +ve	$\Rightarrow$ no overflow
x +ve	y +ve	r -ve	$\Rightarrow$ overflow
x -ve	y -ve	r +ve	$\Rightarrow$ overflow
x -ve	y -ve	r -ve	$\Rightarrow$ no overflow

2. **action**, e.g., **clamp** (or **saturate**) the result to the largest magnitude representable in n bits.

Notes:

Conclusions

Notes:

► Take away points:

1. Computer arithmetic is a foundational (sub-)field of computer science:
 - it's a broad topic with a rich history,
 - there's usually a large design space of potential approaches,
 - they're often easy to understand at an intuitive, high level,
 - correctness and efficiency of resulting low-level solutions is vital and challenging.
2. The strategy we've employed is important and (fairly) general-purpose:
 - explore and understand an approach in theory,
 - translate, formalise, and generalise the approach into an algorithm,
 - translate the algorithm, e.g., into circuit,
 - refine (or select) the circuit to satisfy any design constraints.

Additional Reading

- ▶ [Wikipedia: Computer Arithmetic](https://en.wikipedia.org/wiki/Category:Computer_arithmetic). URL: https://en.wikipedia.org/wiki/Category:Computer_arithmetic.
- ▶ D. Page. “Chapter 7: Arithmetic and logic”. In: *A Practical Introduction to Computer Architecture*. 1st ed. Springer, 2009.
- ▶ B. Parhami. “Part 2: Addition/subtraction”. In: *Computer Arithmetic: Algorithms and Hardware Designs*. 1st ed. Oxford University Press, 2000.
- ▶ W. Stallings. “Chapter 10: Computer arithmetic”. In: *Computer Organisation and Architecture*. 9th ed. Prentice Hall, 2013.
- ▶ A.S. Tanenbaum and T. Austin. “Section 3.2.2: Arithmetic circuits”. In: *Structured Computer Organisation*. 6th ed. Prentice Hall, 2012.

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References

- [1] [Wikipedia: Computer Arithmetic](https://en.wikipedia.org/wiki/Category:Computer_arithmetic). URL: https://en.wikipedia.org/wiki/Category:Computer_arithmetic (see p. 61).
- [2] D. Page. “Chapter 7: Arithmetic and logic”. In: *A Practical Introduction to Computer Architecture*. 1st ed. Springer, 2009 (see p. 61).
- [3] B. Parhami. “Part 2: Addition/subtraction”. In: *Computer Arithmetic: Algorithms and Hardware Designs*. 1st ed. Oxford University Press, 2000 (see p. 61).
- [4] W. Stallings. “Chapter 10: Computer arithmetic”. In: *Computer Organisation and Architecture*. 9th ed. Prentice Hall, 2013 (see p. 61).
- [5] A.S. Tanenbaum and T. Austin. “Section 3.2.2: Arithmetic circuits”. In: *Structured Computer Organisation*. 6th ed. Prentice Hall, 2012 (see p. 61).

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