

► **Concept:** consider

$$\begin{array}{ccc} \hat{x} & \mapsto & x \\ \hat{y} & \mapsto & y \end{array}$$

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$$\begin{array}{lll} \hat{x} & \mapsto & x \\ \hat{y} & \mapsto & y \\ \hat{r} & \mapsto & r = x + y \end{array}$$

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$$\begin{array}{rcl}
 \hat{x} & \mapsto & x \\
 \hat{y} & \mapsto & y \\
 f(\hat{x}, \hat{y}) = \hat{r} & \mapsto & r = x + y
 \end{array}$$

where f

1. has an action on $\hat{x}$ and $\hat{y}$ compatible with that of $+$ on x and y :
 - accepts n -bit
 - **addend** $\hat{x}$, and
 - **addend** $\hat{y}$
 as input, and
 - produces an $(n + 1)$ -bit **sum** $\hat{r}$ as output,
2. is a Boolean function:

$$f : \{0, 1\}^n \times \{0, 1\}^n \rightarrow \{0, 1\}^{n+1}$$

- **Agenda:** produce a design(s) for f , which
 1. functions correctly, and
 2. satisfies pertinent quality metrics (e.g., is efficient in time and/or space).

Part 1: addition in theory (1)

► Concept:

Example ($b = 10$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto \quad 1 \ 0 \ 7 \\ y & = & 14_{(10)} & \mapsto \quad 0 \ 1 \ 4 \ + \\ c & = & & \\ r & = & & \end{array}$$

Example ($b = 2$)

$$\begin{array}{rcll} x & = & 107_{(10)} & \mapsto \quad 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1 \\ y & = & 14_{(10)} & \mapsto \quad 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ + \\ c & = & & \\ r & = & & \end{array}$$

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1. this process matches our understanding of manual, “school-book” addition, *and*
2. the same process applies, irrespective of b .

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Part 2: addition in practice: an algorithm (1)

Algorithm

Input: Two unsigned, n -digit, base- b integers x and y , and a 1-digit carry-in $c_i \in \{0, 1\}$

Output: An unsigned, n -digit, base- b integer $r = x + y$, and a 1-digit carry-out $co \in \{0, 1\}$

```
1  $r \leftarrow 0, c_0 \leftarrow c_i$ 
2 for  $i = 0$  upto  $n - 1$  step  $+1$  do
3    $r_i \leftarrow (x_i + y_i + c_i) \bmod b$ 
4   if  $(x_i + y_i + c_i) < b$  then  $c_{i+1} \leftarrow 0$  else  $c_{i+1} \leftarrow 1$ 
5 end
6  $co \leftarrow c_n$ 
7 return  $r, co$ 
```

Part 2: addition in practice: an algorithm (2)

Example

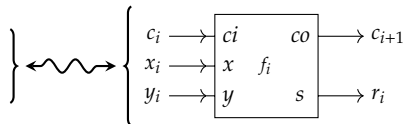
i	x_i	y_i	c_i	r	$x_i + y_i + c_i$	c_{i+1}	r_i	r'
				$\langle 0, 0, 0 \rangle$				$\langle 0, 0, 0 \rangle$
0	7	4	0	$\langle 0, 0, 0 \rangle$	11	1	1	$\langle 1, 0, 0 \rangle$
1	0	1	1	$\langle 1, 0, 0 \rangle$	2	0	2	$\langle 1, 2, 0 \rangle$
2	1	0	0	$\langle 1, 2, 0 \rangle$	1	0	1	$\langle 1, 2, 1 \rangle$
			0	$\langle 1, 2, 1 \rangle$				

Part 3: addition in practice: a circuit (1)

► Idea:

1. for $b = 2$, it's clear from the algorithm that

```
3  $r_i \leftarrow (x_i + y_i + c_i) \bmod b$ 
4 if  $(x_i + y_i + c_i) < b$  then  $c_{i+1} \leftarrow 0$  else  $c_{i+1} \leftarrow 1$ 
```



2. the loop body is therefore analogous to a Boolean function

$$f_i : \{0, 1\}^3 \rightarrow \{0, 1\}^2$$

specified by the following truth table

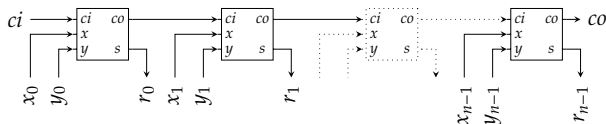
ci	x	y	co	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Part 3: addition in practice: a circuit (1)

► Idea:

- the loop bound is fixed, i.e., n is some known constant, so we can unroll it to yield

Circuit



which, now read left-to-right, mirrors the algorithm:

- the i -th instance f_i implements the i -th loop iteration,
- the connection, or **carry chain** between instances captures c ,
- those instances are termed **full adder cells**,
- this combination of them is termed a **ripple-carry adder**.

Part 3: addition in practice: a circuit (2)

► Beware:

- the magnitude of $r = x + y$ can exceed what we can represent via $\hat{r}$:

$\hat{x}$ and $\hat{y}$ are *unsigned*, and there is a carry-out $\Rightarrow$ **carry** condition
 $\hat{x}$ and $\hat{y}$ are *signed*, and the sign of $\hat{r}$ is incorrect $\Rightarrow$ **overflow** condition

- to cope, we typically

1. detect the condition,
2. potentially take some action (e.g., try to “fix” the result somehow),
3. potentially signal the condition somehow (e.g., via a status register or some form of exception).

Part 3: addition in practice: a circuit (3)

Example

Consider use of an *unsigned* representation:

$$\begin{array}{rcll} x & = & 15_{(10)} & \mapsto & \begin{array}{cccc} 1 & 1 & 1 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} + \\ c & = & & & \begin{array}{cccc} \hline 1 & 1 & 1 & 1 \\ \hline 0 & 0 & 0 & 0 \end{array} \\ r & = & 0_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 0 \end{array} \end{array}$$

Here, the carry-out indicates an error: the correct result $r = 16$ is too large for $n = 4$ bits.

► Note that

1. **detection**:

$$\begin{array}{ll} c_n = CO = 0 & \Rightarrow \text{no carry} \\ c_n = CO = 1 & \Rightarrow \text{carry} \end{array}$$

2. **action**, e.g., **truncate** the result to n bits.

Part 3: addition in practice: a circuit (4)

Example

Consider use of a *signed* representation:

$$\begin{array}{rcll} x & = & -1_{(10)} & \mapsto & \begin{array}{cccc} 1 & 1 & 1 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\ c & = & & & \begin{array}{cccc} 1 & 1 & 1 & 0 \end{array} \\ r & = & 0_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 0 \end{array} \end{array} +$$

Irrespective of the carry-out, the signs of inputs and output make sense: there is no overflow, so $r = 0$ is correct.

Example

Consider use of a *signed* representation:

$$\begin{array}{rcll} x & = & 7_{(10)} & \mapsto & \begin{array}{cccc} 0 & 1 & 1 & 1 \end{array} \\ y & = & 1_{(10)} & \mapsto & \begin{array}{cccc} 0 & 0 & 0 & 1 \end{array} \\ c & = & & & \begin{array}{cccc} 0 & 1 & 1 & 0 \end{array} \\ r & = & -8_{(10)} & \mapsto & \begin{array}{cccc} 1 & 0 & 0 & 0 \end{array} \end{array} +$$

Irrespective of the carry-out, the signs of inputs and output make no sense: there is an overflow, so $r = -8$ is incorrect.

► Note that

1. **detection**:

x +ve	y -ve	$\Rightarrow$	no overflow
x -ve	y +ve	$\Rightarrow$	no overflow
x +ve	y +ve	r +ve	$\Rightarrow$ no overflow
x +ve	y +ve	r -ve	$\Rightarrow$ overflow
x -ve	y -ve	r +ve	$\Rightarrow$ overflow
x -ve	y -ve	r -ve	$\Rightarrow$ no overflow

2. **action**, e.g., **clamp** (or **saturate**) the result to the largest magnitude representable in n bits.

► Take away points:

1. Computer arithmetic is a foundational (sub-)field of computer science:
 - it's a broad topic with a rich history,
 - there's usually a large design space of potential approaches,
 - they're often easy to understand at an intuitive, high level,
 - correctness and efficiency of resulting low-level solutions is vital and challenging.
2. The strategy we've employed is important and (fairly) general-purpose:
 - explore and understand an approach in theory,
 - translate, formalise, and generalise the approach into an algorithm,
 - translate the algorithm, e.g., into circuit,
 - refine (or select) the circuit to satisfy any design constraints.

Additional Reading

- ▶ *Wikipedia: Computer Arithmetic*. URL: https://en.wikipedia.org/wiki/Category:Computer_arithmetic.
- ▶ D. Page. “Chapter 7: Arithmetic and logic”. In: *A Practical Introduction to Computer Architecture*. 1st ed. Springer, 2009.
- ▶ B. Parhami. “Part 2: Addition/subtraction”. In: *Computer Arithmetic: Algorithms and Hardware Designs*. 1st ed. Oxford University Press, 2000.
- ▶ W. Stallings. “Chapter 10: Computer arithmetic”. In: *Computer Organisation and Architecture*. 9th ed. Prentice Hall, 2013.
- ▶ A.S. Tanenbaum and T. Austin. “Section 3.2.2: Arithmetic circuits”. In: *Structured Computer Organisation*. 6th ed. Prentice Hall, 2012.

References

- [1] [Wikipedia: Computer Arithmetic](https://en.wikipedia.org/wiki/Category:Computer_arithmetic). URL: https://en.wikipedia.org/wiki/Category:Computer_arithmetic (see p. 28).
- [2] D. Page. “Chapter 7: Arithmetic and logic”. In: *A Practical Introduction to Computer Architecture*. 1st ed. Springer, 2009 (see p. 28).
- [3] B. Parhami. “Part 2: Addition/subtraction”. In: *Computer Arithmetic: Algorithms and Hardware Designs*. 1st ed. Oxford University Press, 2000 (see p. 28).
- [4] W. Stallings. “Chapter 10: Computer arithmetic”. In: *Computer Organisation and Architecture*. 9th ed. Prentice Hall, 2013 (see p. 28).
- [5] A.S. Tanenbaum and T. Austin. “Section 3.2.2: Arithmetic circuits”. In: *Structured Computer Organisation*. 6th ed. Prentice Hall, 2012 (see p. 28).